**Lab00: To be the familiar with VHDL simulation**

1 Getting started

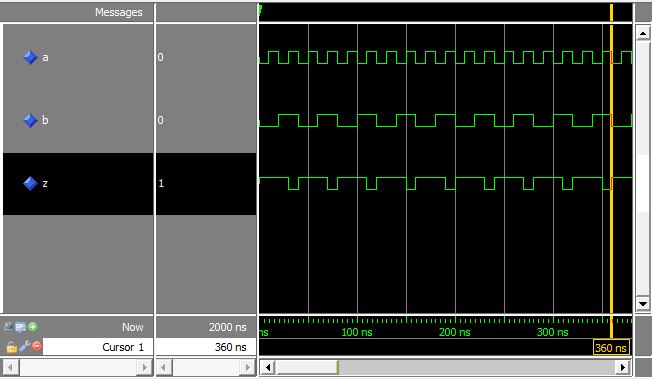
* The VHDL design style used in the file mux2in1b.vhd is data flow
* The VHDL design style used in the file mux2in1b\_3state.vhd is behavioral
* The two simulation results are same.

2 NAND gate modeling example

* Truth table NAND gate: Z= X.Y

|  |  |  |
| --- | --- | --- |
| X | Y | Z |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

* Simulation results:

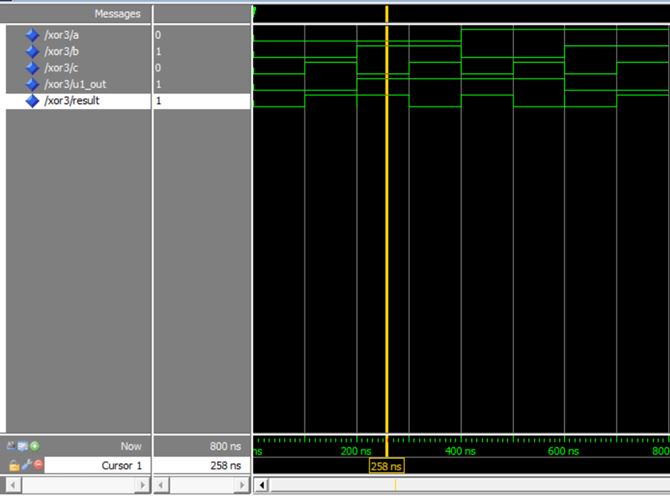


3 Xor3 gate in different design styles

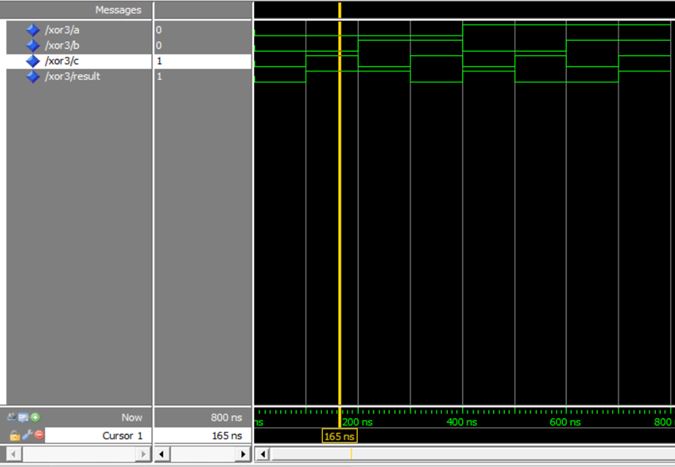
* Truth table Xor3 gate: Z = BC + ABC + ABC

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Z |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

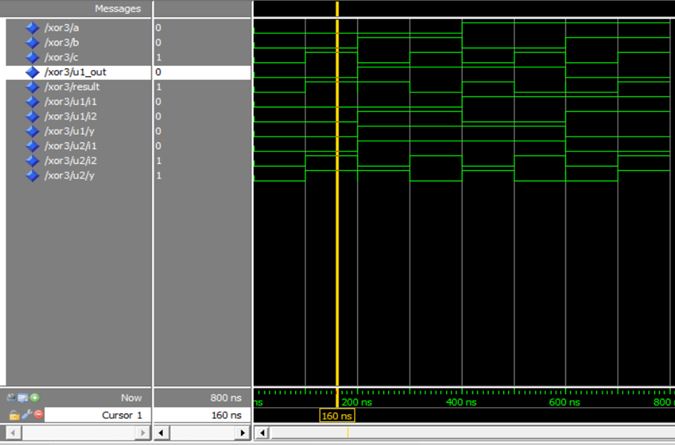
3.1 Dataflow Architecture



3.2 Structural Architecture



3.3 Behavioral structure



* The result of both 3 design style are same.